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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application: In Cheol RYU
Serial No.: 10/034,497 GRP ART UNIT: 2814
Filed: December 29, 2001 Ex.: QUACH, T.
For: METHOD OF FORMING A CONTACT FOR A SEMICONDUCTOR DEVICE

CLAIM-CLEAN VERSION

Please cancel Claims 6 and 15 without prejudice.

Please replace Claims 1, 4-5, 10, and 13-14 with the clean version of the amended Claims 1, 4-5, 10, and 13-14 as set forth below:

1. (Twice Amended) A method of forming a contact for a semiconductor device, comprising the steps of:

forming a first interlayer dielectric layer on a silicon substrate;

forming a conductive material pattern on a portion of the first interlayer dielectric layer;

forming a second interlayer dielectric layer over the first interlayer dielectric layer and over the conductive material pattern;

forming first and second contact holes by selectively removing the second and the first interlayer dielectric layers so as to respectively expose a portion of the conductive material pattern and a portion of the silicon substrate;

forming a glue layer on the first and the second interlayer dielectric layers including over the first and the second contact holes, the glue layer being made up of both Ti and TiN layers by using a TDMET source;

treating plasma on the glue layer using N_2 or H_2, alone or in combination, during the step of forming the glue layer; and

filling the first and the second contact holes with a tungsten layer by forming the tungsten layer on the glue layer.

4. (Once Amended) The method of claim 1, wherein the glue layer is deposited to a thickness of less than about 400Å by using a TDMAT or $TiCl_4$ source instead of the TDMET source.

5. (Twice Amended) The method of claim 4, wherein a plasma treatment is continued after the formation of the glue layer.

10. (Twice Amended) A method of forming a contact for a semiconductor device, comprising the steps of:

forming a first interlayer dielectric layer on a silicon substrate;

forming a conductive material pattern on a portion of the first interlayer dielectric layer, wherein the conductive material pattern has a lower etch rate than the first interlayer dielectric layer;

forming a second interlayer dielectric layer over the first interlayer dielectric layer and over the conductive material pattern;

selectively and sequentially removing the second and the first interlayer dielectric layers so as to form first and second contact holes, wherein the second contact hole has a depth greater than the first contact hole, wherein the first contact hole exposes a portion of the conductive material pattern, and wherein the second contact hole exposes a portion of the silicon substrate;

forming a glue layer made up of both Ti and TiN layers by using a TDMAT source on the first and the second interlayer dielectric layers including over the first and the second contact holes;

treating plasma on the glue layer using N_2 or H_2, alone or in combination, during the step of forming the glue layer; and

forming a tungsten layer on the CVD TiN layer so as to fill the first and the second contact holes.

13. (Once Amended) The method of claim 10, wherein the CVD TiN layer is deposited with a thickness of less than about 400Å by using a TDMAT or $TiCl_4$ source instead of the TDMET source.

14. (Twice Amended) The method of claim 13, wherein a plasma treatment is carried after the formation of the glue layer.